DC-40 GHZ AND 20-40 GHZ MMIC SPDT SWITCHES

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ABSTRACT

Monolithic GaAs SPDT switches operating from dc to 40 GHz and 20 to 40 GHz have been demonstrated. The switches use MESFETs with the same characteristics as a mm-wave amplifier to allow for ease of integration in the future. The gate length is 0.35 microns, and ion implanted material is used. The 20-40 GHz switch uses a combination of shunt FETs and quarter-wave transformers. Better than 2 dB insertion loss and 25 dB isolation have been achieved. The dc-40 GHz switch uses a combination of series and shunt FETs. Better than 3 dB insertion loss and 23 dB isolation have been achieved. Power handling and switching speed have also been measured for both switch types.

INTRODUCTION

Broadband GaAs MMIC switches have been demonstrated over large bandwidths. A bandwidth greater than one octave (6-19 GHz) has been demonstrated using shunt FETs as switching elements [1]. The present work includes a similar design intended for millimeter wave operation. Operation from dc to 20 GHz has been achieved with a combination of series and shunt FET switching elements [2] and from 2 to 18 GHz with series and shunt PIN diodes switching elements [3]. The present work includes a dc-40 GHz switch incorperating features from both these topologies. Both series and shunt FETs are used and operation has been extended to millimeter waves.

The use of FETs as switching elements is well documented [4]. When the gate is biased at 0 volts (the "on" state), a small resistance is present between the source and drain. When the gate is biased beyond pinch-off (the "off" state), the source and drain are capacitively coupled. Resistive elements are also present. In order to minimize the effect of the "off" state capacitance in a broadband switch, the FETs are generally inserted in an artificial transmission line [1].

CIRCUIT STRUCTURES

The topology of the 20-40 GHz SPDT switch is indicated in figure 1. Switching FETs are used in a shunt configuration in conjunction with quarter wave transformers. The circuit is comprised of two equal but independently biased arms. In normal operation, one arm passes the signal (the "on arm") and the other arm isolates the signal (the "off arm"). The FETs in "on arm" are pinched-off, and act primarily as shunt capacitances. The FETs are connected through series inductive lines. The combination of the

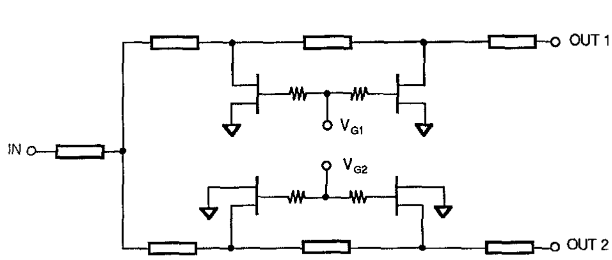

Figure 1. Topology of the 20-40 GHz SPDT Switch.

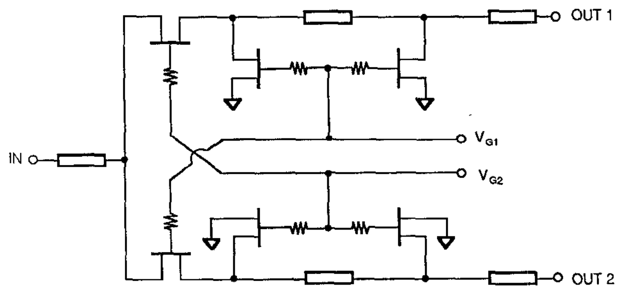

Figure 2. Topology of the dc-40 GHz SPDT Switch.

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series inductance of the lines and the shunt capacitance of the FETs forms an artificial transmission line. The FETs in the "off arm" are biased in the "on" state and act as small shunt resistances. They approximate a short circuit. The quarter-wave transformer is used to transform the short into an open, preventing the "off arm" from loading down the "on arm".

To achieve adequate switching performance over a broader bandwidth the topology in figure 2 is used. The quarter wave transformers from figure 1 are replaced by series FETs. The series FET in the "on arm" is biased "on" and acts as a small resistance, allowing the signal to pass (with some small attenuation). The shunt FETs

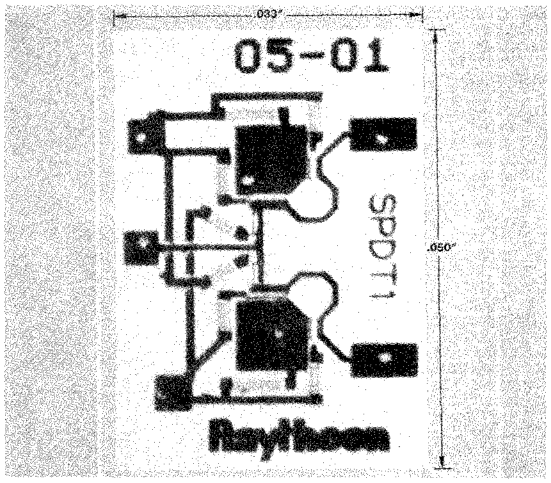

Figure 3. Photograph of the dc-40 GHz SPDT Switch.

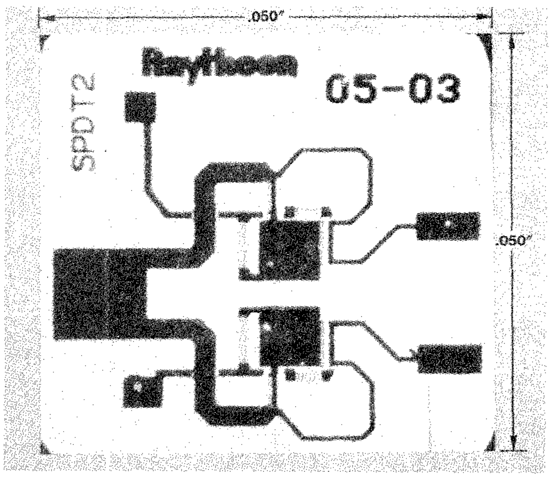

Figure 4. Photograph of the 20-40 GHz SPDT Switch.

in the "on arm" function the same as in figure 1. The series FET in the "off arm" is pinched off and acts primarily as a small capacitance. This capacitance is essentially grounded through the shunt FETs, and thus presents additional capacitive loading on the "on arm". The additional capacitive loading must also be incorporated into the artificial transmission line. Isolation is primarily provided by the shunt FETs in the "off arm", particularly at high frequencies where the series FETs provide very little isolation.

IMPLEMENTATION

The circuits have been fabricated as GaAs MMICs. Ion implantation is used to dope the FETs to 3×10^{17} cm^{-3} with a contact layer of 1×10^{18} cm^{-3}. The gates are 0.35 microns long. Polyimide passivation is used. Gate bias is provided through FET type (open gate) resistors. No other resistor types and no capacitors are used. Transmission lines are realized with 3 micron thick plated gold, with a minimum line width of 10 microns. The substrate is thinned to 100 microns and 50 micron square via holes are plasma etched. The completed dc-40 GHz switch is shown in figure 3. It has a total gate periphery of 430 microns. The completed 20-40 GHz switch is shown in figure 4. It has a total gate periphery of 560 microns. The switches contain all bias circuitry on chip and are very small. The dc-40 GHz circuit is only 33 x 50 mils (0.84 x 1.27 mm). The 20-40 GHz circuit is only 50 x 50 mils (1.27 x 1.27 mm).

PERFORMANCE

The measured small signal performance of the dc-40 GHz switch is shown in figure 5. Insertion loss is between 2 dB and 3 dB from dc to 40 GHz. Isolation is in excess of 23 dB from dc to 40 GHz. Isolation is lowest at 40 GHz and increases continually as frequency decreases. Return loss is 10 dB or better over the dc-40 GHz band with the exception of occasional peaks to 9 dB and 8 dB. Small signal performance for the 20-40 GHz switch is shown in figure 6. From 18-40 GHz the insertion loss is less than 2 dB. The isolation is 25 dB over most of the band, degrading to 24 dB at the very low band edge. The return loss at the input is better than 10 dB over the band. Return loss averages 7 dB at the output.

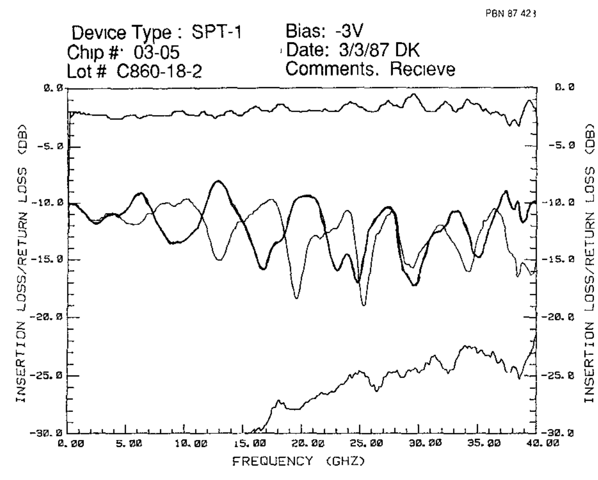

Figure 5. Small Signal Performance of dc-40 GHz SPDT Switch.

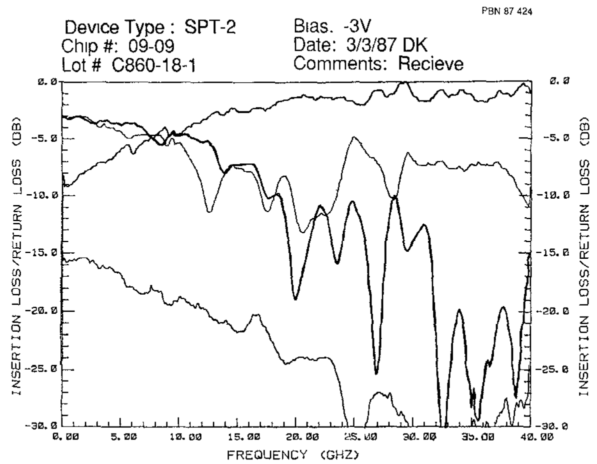

Figure 6. Small Signal Performance of 20-40 GHz SPDT Switch.

Insertion loss and isolation have also been measured at power levels up to 25 dBm (300 mw). Figure 7 shows insertion loss and isolation transfer curves for the dc-40 GHz switch at various frequencies across the band. Insertion loss starts degrading significantly above 18 dBm (60 mw). This is caused by current limiting in the series FETs. The isolation degrades more gradually. At 18 dBm the isolation does not yet show significant degradation except at 40 GHz. The degradation in isolation is caused by current limiting in the shunt FETs. Figure 8 shows the power transfer curves for insertion loss and isolation for the 20-40 GHz switch. Insertion loss is not significantly degraded until 23 dBm (200 mw). Since there are no series FETs, power

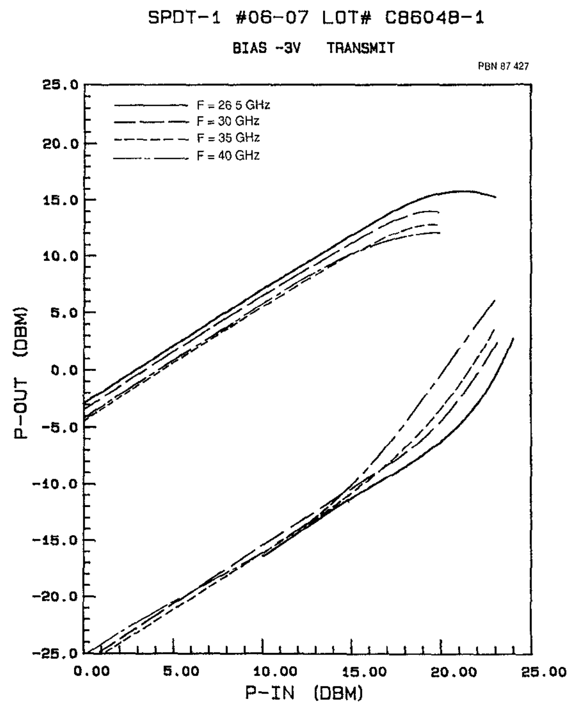

Figure 7. Insertion Loss and Isolation Transfer Curves for dc-40 GHz SPDT Switch.

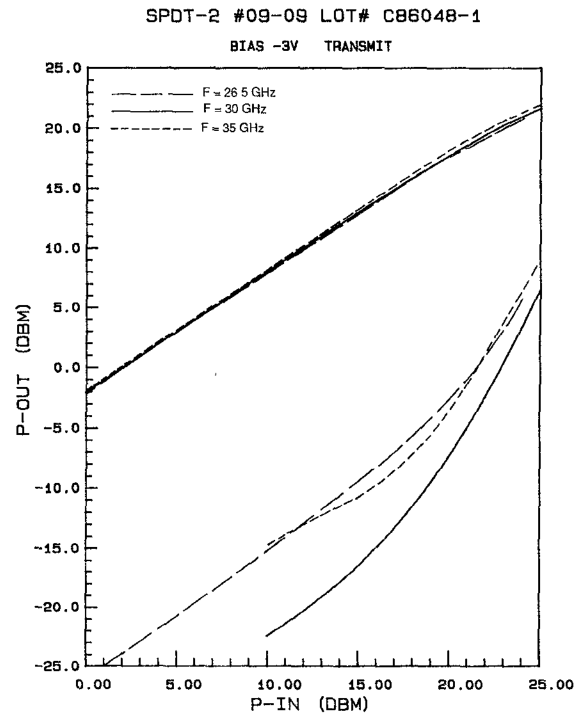

Figure 8. Insertion Loss and Isolation Transfer curves for 20-40 GHz SPDT Switch.

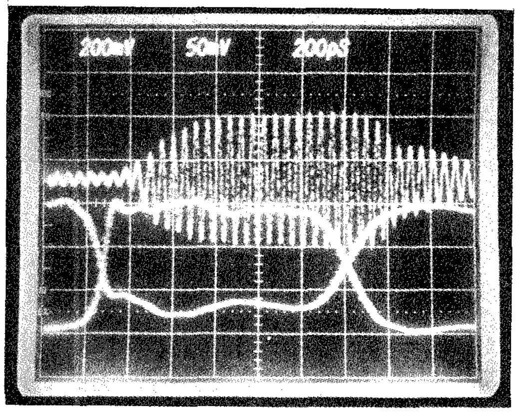

Figure 9. Switching Speed for dc-40 GHz SPDT Switch.

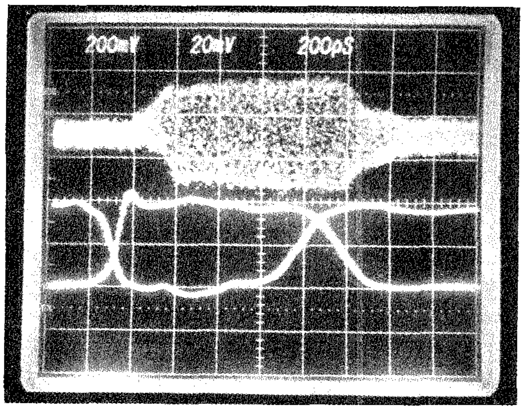

Figure 10. Switching Speed for 20-40 GHz SPDT Switch.

starts to be limited by voltage swings across the shunt FETs. Isolation degrades significantly for power levels above 20 dBm (100 mw). Isolation degrades because of current limiting in the shunt FETs.

Switching speed has been measured for both switches with a 18 GHz rf signal. Figure 9 shows the detected rf output from the dc-40 GHz switch in the top trace and the complementary bias inputs in the bottom trace. The turn-on time is less than 500 psec, the turn-off time is less than 800 psec. Figure 10 shows the switching speed for the 20-40 GHz switch. The turn-on time is less than 300 psec and the turn-off time is less than 400 psec. The 20-40 GHz switch has lower resistance in the bias network, and thus switches faster.

SUMMARY

Two millimeter wave switches has been demonstrated, one covering 20-40 GHz, the other dc-40 GHz. Insertion losses are better than 2 dB and 3 dB respectively. Isolations are 25 dB. Switching speeds are all under 1 nsec. Power handling capabilities between 60 and 100 mw have been demonstrated.

In order to achieve millimeter wave operation, small FET peripheries were used. Since power limiting is caused by FET current limiting, only moderate power handling ability has been demonstrated. Relatively low current FETs were used so that the switches would be compatible with an millimeter wave amplifier [5]. I_{dss} for these FETs is 220 ma/mm. Higher power handling would readily be achieved with higher current FETs.

ACKNOWLEDGEMENTS

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